TEMIC

Siliconix

TN0201T

N-Channel Enhancement-Mode MOS Transistor

Product Summary

$V_{(BR)DSS}$ Min (V)	$r_{DS(on)}$ Max (Ω)	$V_{GS(th)}$ (V)	I_D (A)
20	1.0 @ V_{GS} = 10 V	1.0 to 3.0	0.3
	1.4 @ V_{GS} = 4.5 V		

Features

- Low On-Resistance: 0.75 Ω
- Low Threshold: <1.75 V
- Low Input Capacitance: 65 pF
- Fast Switching Speed: 15 ns
- Low Input and Output Leakage

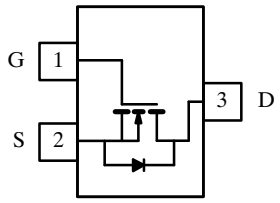
Benefits

- Low Offset Voltage
- Low-Voltage Operation
- Easily Driven Without Buffer
- High-Speed Circuits
- Low Error Voltage

Applications

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

TO-236
(SOT-23)



Top View

TN0201T (N1)*

*Marking Code for TO-236

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	0.3	A
	T_A = 70°C		0.24	
Pulsed Drain Current		I_{DM}	0.75	
Power Dissipation	T_A = 25°C	P_D	0.2	W
	T_A = 70°C		0.128	
Maximum Junction-to-Ambient		R_{thJA}	625	°C/W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Notes
a. Pulse width limited by maximum junction temperature.

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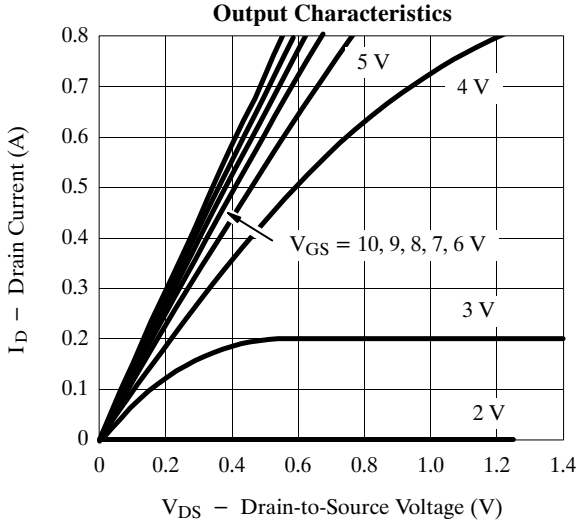
Specifications[a]

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ[b]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	20	40		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA	1.0	1.90	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		V_{DS} = 14 V, V_{GS} = 0 V, T_J = 55°C			10	
On-State Drain Current[c]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	0.5	0.75		A
Drain-Source On-Resistance[c]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.1 A		1	1.4	Ω
		V_{GS} = 10 V, I_D = 0.3 A		0.75	1.0	
Forward Transconductance[c]	g_{fs}	V_{DS} = 10 V, I_D = 0.2 A		450		mS
Diode Forward Voltage	V_{SD}	I_S = 0.3 A, V_{GS} = 0 V		0.85		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 16 V, V_{GS} = 10 V, I_D ≅ 0.3 A		1400		pC
Gate-Source Charge	Q_{gs}			300		
Gate-Drain Charge	Q_{gd}			200		
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		65		pF
Output Capacitance	C_{oss}			35		
Reverse Transfer Capacitance	C_{rss}			6		
Switching[b, d]						
Turn-On Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 50 Ω I_D ≅ 0.3 A, V_{GEN} = 10 V R_G = 6 Ω		5		ns
	t_r			10		
Turn-Off Time	$t_{d(off)}$			12		
	t_f			6		

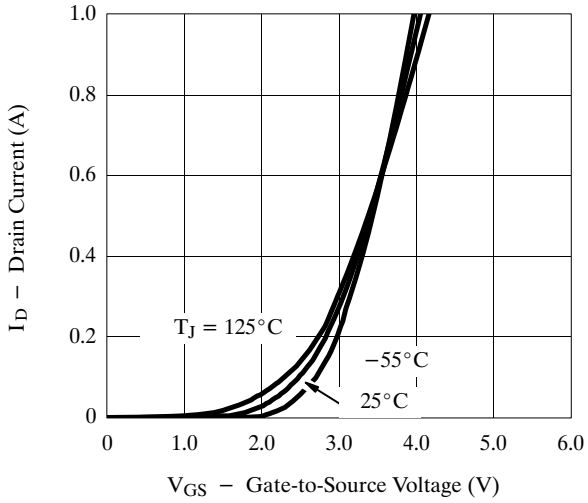
Notes
a. T_A = 25°C unless otherwise noted. VNBP02
b. For DESIGN AID ONLY, not subject to production testing.
c. Pulse test: PW ≤ 300 µs duty cycle ≤ 2%.
d. Switching time is essentially independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

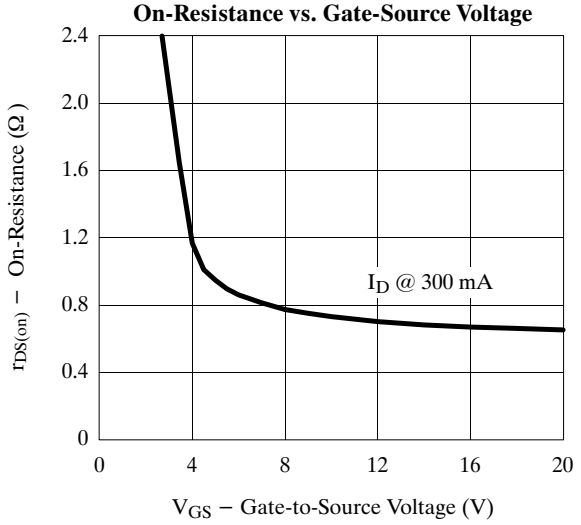
Output Characteristics



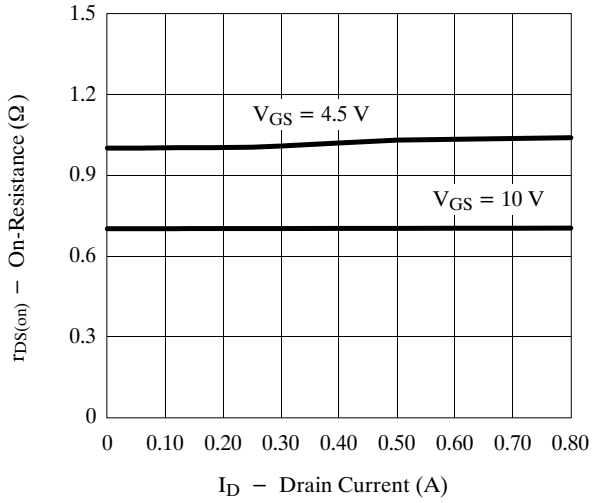
Transfer Characteristics



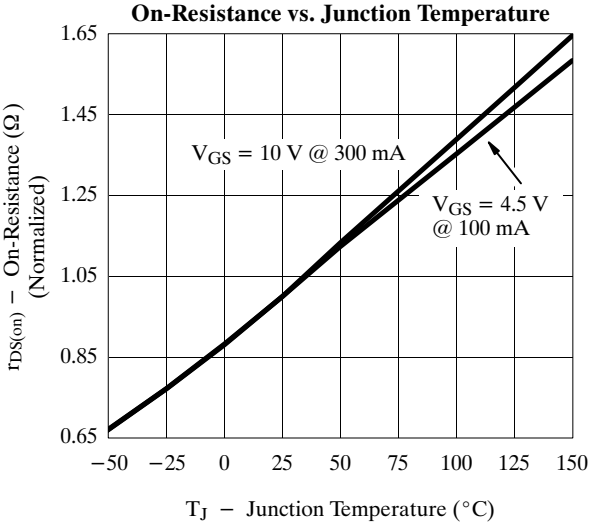
On-Resistance vs. Gate-Source Voltage



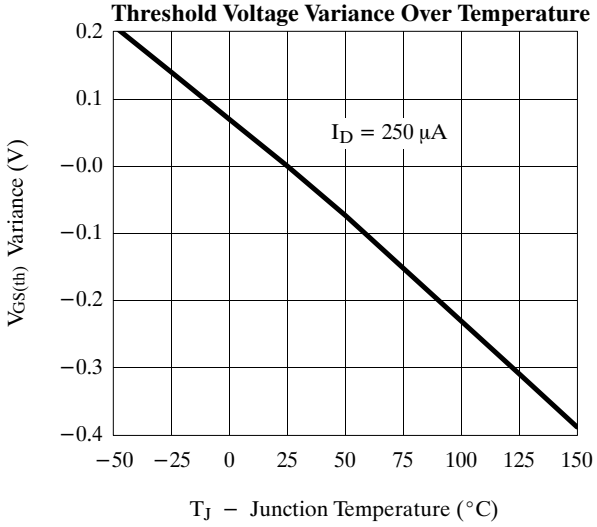
On-Resistance vs. Drain Current



On-Resistance vs. Junction Temperature



Threshold Voltage Variance Over Temperature



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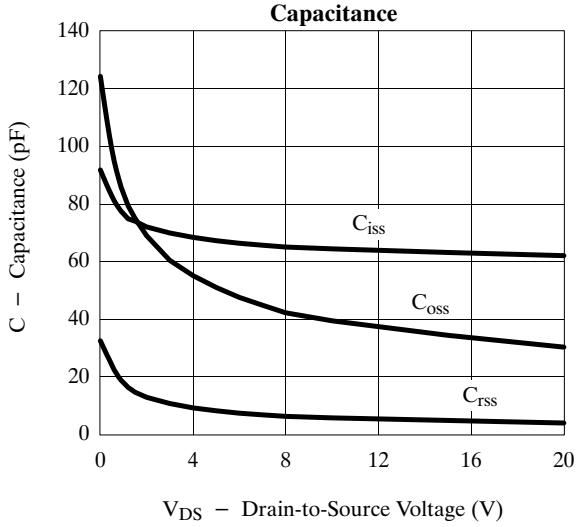
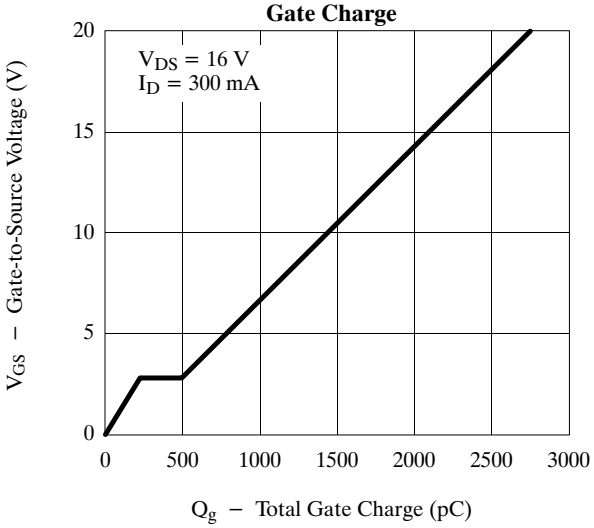
Typical Characteristics (25°C Unless Otherwise Noted)

Capacitance



Gate Charge



Source-Drain Diode Forward Voltage